

U.S.S.N. 10,791,606

Claim Amendments

Please amend claims 1, 2, and 4 as follows:

Please cancel claims 15-27 as follows:

Please add new claims 28-40 as follows:

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Claims as Amended

1. (currently amended) A method for forming an improved fuse link structure comprising the steps of:

providing spaced apart first and second metal interconnect structures each respectively electrically interconnected to form fuse interconnect portions extending through a plurality of dielectric insulating layers including an uppermost metal interconnect layer;

forming a first dielectric insulating layer over the uppermost metal interconnect layer;

forming at least a second dielectric insulating layer over the first dielectric insulating layer;

forming first and second trench openings in said at least a second dielectric insulating layer to respectively overlie the first and second metal interconnect structures;

forming first and second via openings extending from a bottom portion of the respective first and second trench ~~time~~

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openings through the first dielectric insulating layer to respectively overlie the respective first and second metal interconnect structures while simultaneously etching away a predetermined thickness of the at least a second dielectric insulating layer spanning an area extending between and overlying the first and second via trench openings; and,

filling the first and second via openings and first and second trench ~~line~~ openings with a metal to form a metal fuse link electrically interconnecting the first and second metal interconnect structures to form a metal fuse link portion comprising the predetermined thickness.

2. (currently amended) The method of claim 1, wherein the at least a second dielectric insulating layer comprises a lowermost dielectric insulating layer and an uppermost dielectric insulating layer separated by an etch stop layer formed at a level comprising the predetermined thickness.

3. (original) The method of claim 1, wherein etch stop layers are formed to separate the first dielectric insulating layer and the at least a second dielectric insulating layer.

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4. (currently amended) The method of claim 1, wherein a metal interconnect guard ring structure is formed in parallel to surround the fuse link and the fuse interconnect portions, said guard ring structure further to extending downward through at least a portion of the plurality of dielectric insulating layers.

5. (original) The method of claim 1, wherein a bottom anti-reflectance coating (BARC) comprising one of an organic and inorganic material is formed over and contacting an uppermost layer of the at least a second dielectric insulating layer.

6. (original) The method of claim 1, wherein the plurality of dielectric insulating layers comprise a low-K inorganic material selected from the group consisting of fluorine doped silicon oxide, carbon doped silicon oxide, and organo-silane glass (OSG).

7. (original) The method of claim 1, wherein the metal is selected from the group consisting of copper, aluminum, and alloys thereof.

8. (original) The method of claim 7, wherein the metal consists primarily of copper.

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9. (original) The method of claim 8, wherein the step of filling further comprises the steps of:

depositing at least one of a refractory metal and refractory metal nitride to form a barrier layer lining the respective via and trench openings;

depositing a copper seed layer over the barrier layer;

carrying out an electro-chemical deposition process to fill the respective via and trench openings; and

carrying out a chemical mechanical polishing process to remove excess copper overlying respective trench opening levels.

10. (original) The method of claim 1, wherein the predetermined thickness is from about 1500 Angstroms to about 5000 Angstroms.

11. (original) The method of claim 1, wherein the predetermined thickness is from about 2500 Angstroms to about 3500 Angstroms.

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12. (original) The method of claim 1, wherein the first and at least a second dielectric insulating layer are formed of a material selected from the group consisting of undoped silicate glass (USG), CVD silicon oxide, PECVD silicon oxide, and TEOS silicon oxide.

13. (original) The method of claim 1, wherein the etch stop layer is selected from the group consisting of silicon carbide and silicon nitride.

14. (original) The method of claim 1, wherein the at least a second dielectric insulating layer is formed at a thickness of from about 10000 Angstroms to about 40,000 Angstroms.

Claims 15-27 cancelled

28. (new) A method for forming a fuse link structure comprising the steps of:

providing spaced apart first and second metal interconnect structures extending through a plurality of dielectric layers;

forming at least one dielectric layer over said first and

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second interconnect structures;

forming damascene openings through a thickness of said at least one dielectric layer to respectively overlie said first and second interconnect structures while simultaneously removing a predetermined thickness portion of an upper portion of said at least one dielectric layer to span an area extending between said damascene openings.

filling the damascene openings with a metal including said predetermined thickness portion to form a metal fuse link electrically interconnecting the first and second metal interconnect structures to form a metal fuse link portion comprising the predetermined thickness.

29. (new) The method of claim 28, wherein said damascene openings comprise dual damascene openings.

30. (new) The method of claim 28, wherein said at least one dielectric layer comprises at least two dielectric layers.

31. (new) The method of claim 30, further comprising an etch stop layer separating said at least two dielectric layers at about

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said predetermined thickness.

32. (new) The method of claim 28, wherein said damascene openings comprise dual damascene openings wherein a respective via portion and a trench portion are separated by an etch stop layer.

33. (new) The method of claim 28, wherein the predetermined thickness is from about 1500 Angstroms to about 5000 Angstroms.

34. (new) The method of claim 28, wherein the at least one dielectric layer comprising the predetermined thickness is formed at a thickness of from about 10,000 Angstroms to about 40,000 Angstroms.

35. (new) The method of claim 28, wherein said at least one dielectric layer is formed of a material selected from the group consisting of undoped silicate glass (USG), CVD silicon oxide, PECVD silicon oxide, and TEOS silicon oxide.

36. (new) A method for forming a copper fuse link structure for blowing by laser ablation comprising the steps of:

providing spaced apart first and second metal interconnect

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structures extending through a plurality of dielectric layers;

forming a first dielectric layer over said first and second interconnect structures;

forming at least a second dielectric layer over said first dielectric layer;

forming damascene openings through a thickness of said first and at least a second dielectric layer to respectively overlie said first and second interconnect structures while simultaneously removing a predetermined upper thickness portion of said at least a second dielectric layer to form a fuse link opening spanning an area extending between said damascene openings.

filling the damascene openings and fuse link opening with copper to form a copper fuse link electrically interconnecting the first and second metal interconnect structures.

37. (new) The method of claim 36, wherein said damascene openings comprise dual damascene openings.

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38. (new) The method of claim 36, further comprising an etch stop layer separating said at least two dielectric layers at about said predetermined thickness.

39. (new) The method of claim 36, wherein said damascene openings comprise dual damascene openings wherein a respective via portion and a trench portion are separated by an etch stop layer.

40. (new) The method of claim 36, wherein said at least one dielectric layer is formed of a material selected from the group consisting of undoped silicate glass (USG), CVD silicon oxide, PECVD silicon oxide, and TEOS silicon oxide.